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| 10/725,326 | 12/01/2003 | Fwu-Iuan Hshieh | GS 145 D1 | 2693 |

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| EXAMINER | |
|---|---|
| CAO, PHAT X | |
| **ART UNIT** | **PAPER NUMBER** |
| 2814 | |

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| **Office Action Summary** | **Application No.** 10/725,326 | **Applicant(s)** HSHIEH ET AL. | |
|---|---|---|---|
| | **Examiner** Phat X. Cao | **Art Unit** 2814 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 20 October 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 24,31 and 32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 24,31 and 32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The cancellation of claims 1-23 and 25-30 in Paper filed 10/20/04 is acknowledged.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al (US. 5,925,911) in view of Kubo (US. 5,463,241).

Okabe (Figs. 3-10) discloses a method of forming a trench DMOS transistor device comprising: providing a substrate 1 of a first conductivity type (N+), the substrate acting as a common drain region for the device (column 4, lines 3-4); depositing an epitaxial layer 2 of the first conductivity type (N-) over the substrate, the epitaxial layer 2 (N-) having a lower majority carrier concentration than the substrate 1 (N+); forming a body region 40 of a second conductivity type (P) within an upper portion of the epitaxial layer 2; etching a trench 60 extending into the epitaxial layer 2from an upper surface of the epitaxial layer 2 (Fig. 7); forming an insulating layer 6 lining at least a portion of the trench (see Fig. 10 and column 5, lines 55-60); forming a conductive region 7 within the trench adjacent the insulating layer; forming a source region 5 of the first conductivity type (N+) within an upper portion of the body region 40 and

adjacent the trench; forming a low resistivity deep region 31 of N+ extending into the device from an upper surface of the epitaxial layer 2, the deep region 2 acting to provide electrical contact with the substrate 1; and forming a source contact 9 adjacent an upper surface of the source region 5, and a gate contact adjacent an upper surface of the conductive region 7 in a termination region remote from the source region 7.

Okabe does not disclose the drain contact deep region 31 formed by a metal extending from an upper surface of the epitaxial layer 2 through the epitaxial layer 2.

However, Kubo (Figs. 6B-6D) teaches the forming of a metallic source/drain contact and a metallic gate contact (column 5, lines 1-6) and the forming of a metal contact deep region 101 comprising a low resistivity material such as doped polycrystalline silicon and refractory metals (column 4, lines 56-59), wherein the deep region 101 is formed by a process comprising etching a deep trench 200 (Fig. 6B) that extends into the device from an upper surface of the epitaxial layer 1b (P-) and depositing doped polycrystalline silicon or refractory metals 101 within the deep trench 200. Accordingly, it would have been obvious to modify the process of Okabe by forming the drain contact deep region 31 with the process as set forth above, because as taught by Kubo, such modified process would form the deep region with the refractory metal materials for reducing source/drain resistance, improving high frequency gains and improving heat dissipation characteristics (column 5, lines 45-55).

4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish et al (US. 5,674,766) in view of Kubo (US. 5,463,241).

,Darwish (Fig. 3D) discloses a method of forming a conventional trench DMOS transistor device comprising: providing a substrate 120 of a first conductivity type (N=), the substrate 120 acting as a common drain region for the device; depositing an epitaxial layer 111 of the first conductivity type (N) over the substrate 120, the epitaxial layer 111 having a low majority carrier concentration than the substrate 120; forming a body region 114 of a second conductivity type within an upper surface of the epitaxial layer 111; etching a trench extending into the epitaxial layer 111 from an upper surface of the epitaxial layer 111; forming an insulating layer (not labeled) lining at least a portion of the trench; forming a conductive region 102 within the trench adjacent the insulating layer; forming a source region (not labeled) of the first conductivity type (N+) within an upper portion of the body region 114 and adjacent the trench; and forming a metallic source contact 118 (column 1, lines 64-65) adjacent an upper surface of the source region, and a metallic gate contact 121 (column 3, lines 30-31) adjacent an upper surface of the conductive region 102 in a termination region remote from the source region. Darwish's Fig. 13 also teaches the forming of a low resistivity deep region 304 of N+ type extending from an upper surface of the epitaxial layer to the substrate 318 for providing an electrical contact to the drain or the substrate.

Darwish does not disclose the drain contact deep region 304 formed by a metal extending from an upper surface of the epitaxial layer through the epitaxial layer.

However, Kubo (Figs. 6B-6D) teaches the forming of a metallic source/drain contact and a metallic gate contact (column 5, lines 1-6) and the forming of a metal contact deep region 101 comprising a low resistivity material such as doped polycrystalline silicon and refractory metals (column 4, lines 56-59), wherein the deep region 101 is formed by a process comprising etching a deep trench 200 (Fig. 6B) that extends into the device from an upper surface of the epitaxial layer 1b (P-) and depositing doped polycrystalline silicon or refractory metals 101 within the deep trench 200. Accordingly, it would have been obvious to modify the process of Darwish by forming the drain contact deep region 31 with the process as set forth above, because as taught by Kubo, such modified process would form the deep region with the refractory metal materials for reducing source/drain resistance, improving high frequency gains and improving heat dissipation characteristics (column 5, lines 45-55).

5. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al (US. 5,925,911) in view of Williams et al (US. 5,945,709).

Okabe (Figs. 3-10) discloses a method of forming a trench DMOS transistor device comprising: providing a substrate 1 of a first conductivity type (n+), the substrate acting as a common drain region for the device (column 4, lines 3-4); depositing an epitaxial layer 2 of the first conductivity type (n-) over the substrate, the epitaxial layer 2 (n-) having a lower majority carrier concentration

than the substrate 1 (n+); forming a body region 40 of a second conductivity type (p) within an upper portion of the epitaxial layer 2; etching a trench 60 (Fig. 7) extending into the epitaxial layer 2 from an upper surface of the epitaxial layer 2; forming an insulating layer 6 lining at least a portion of the trench; forming a conductive region 7 within the trench adjacent the insulating layer 6; forming a low resistivity deep region 31 of the first conductivity type (n+) by implantation and diffusion (column 5, lines 14-18), the low resistivity deep region 31 extending into the device from an upper surface of the epitaxial layer 2 and acting to provide electrical contact with the substrate 1; and forming a source region 5 of the first conductivity type (n+) within an upper portion of the body region 40 and adjacent the trench 60.

Okabe does not disclose that the step of forming the source region 5 also forms a region of first conductivity type within the low resistivity deep region 31.

However, Williams (Figs. 9A-9D) teaches the forming of a source region of a first conductivity type (n+) within an upper portion of a body region 85 and the forming of a low resistivity deep region 70 extending into the device from an upper surface of an epitaxial layer 72, wherein the step of forming the source region also forms a region of first conductivity (n+) within the low resistivity deep region 70 (also see column 9, lines 4-7). Accordingly, it would have been obvious to modify the process steps of Okabe by forming a region of first conductivity within the deep region 31 at the same step of forming the source region 5 because the process step of forming the diffusion region within the deep region and having the same conductivity with the deep region is well known and

commonly used for providing the low resistance source/drain contact region, as taught by Williams (column 9, lines 4-7).

6. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish et al (US. 5,674,766) in view of Williams et al (US. 5,945,709).

Regarding claim 31, Darwish (Fig. 3D) discloses a method of forming a trench DMOS transistor device comprising: providing a substrate 120 of a first conductivity type (n+), the substrate 120 acting as a common drain region for the device; depositing an epitaxial layer 111 of the first conductivity type (n) over the substrate, the epitaxial layer 111 (n) having a lower majority carrier concentration than the substrate 120 (n+); forming a body region 114 of a second conductivity type (p+) within an upper portion of the epitaxial layer 111; etching a trench extending into the epitaxial layer 111 from an upper surface of the epitaxial layer; forming an insulating layer (not labeled) lining at least a portion of the trench; forming a conductive region 102 within the trench adjacent the insulating layer; forming a low resistivity deep region 304 (not shown in Fig. 3D, see Fig. 13) extending into the device from an upper surface of the epitaxial layer, the deep region acting to provide electrical contact with the substrate; and forming a source region (not labeled) of the firs conductivity type (n+) within an upper portion of the body region 114 and adjacent the trench.

Darwish does not disclose that the step of forming the source region also forms a region of first conductivity type within the low resistivity deep region 304.

However, Williams (Figs. 9A-9D) teaches the forming of a source region of a first conductivity type (n+) within an upper portion of a body region 85 and the

forming of a low resistivity deep region 70 extending into the device from an upper surface of an epitaxial layer 72, wherein the step of forming the source region also forms a region of first conductivity (n+) within the low resistivity deep region 70 (also see column 9, lines 4-7). Accordingly, it would have been obvious to modify the process steps of Darwish by forming a region of first conductivity within the deep region at the same step of forming the source region because the process step of forming the diffusion region within the deep region and having the same conductivity with the deep region is well known and commonly used for providing the low resistance source/drain contact region, as taught by Williams (column 9, lines 4-7).

Regarding claim 32, Williams also teaches that the region of first conductivity (n+) formed within the low resistivity deep region 70 is formed by implantation and diffusion (column 9, lines 4-7).

***Response to Arguments***

7. Applicant argues that the applied references do not suggest the forming of a metal drain contact as claimed.

This argument is not persuasive because the combination of the applied references clearly suggest the invention as claimed. Specifically, Okabe (Fig. 10) and Darwish (Fig. 13) clearly discloses the forming of a drain contact extending from an upper surface of the epitaxial layer through the epitaxial layer and into contact with the substrate (see ground of rejection(s) for more details). And Kubo (Figs. 6B-6D) clearly teaches the forming of a metal source/drain contact 101 extending from an upper surface of the epitaxial layer 1b through the

epitaxial layer 1b and into contact with the substrate 1a for the purpose of reducing source/drain resistance, improving high frequency gains and improving heat dissipation characteristics (column 5, lines 45-55).

Regarding newly submitted claims 31-32, the new reference is applied to show the obviousness of the invention as claimed.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
January 6, 2005

PHAT X. CAO
PRIMARY EXAMINER